

CLAIMS

What is claimed is:

- 1 1. A system for accessing a two way associative data cache having first and
2 second ways, comprising:

3 a clock circuit for selectively applying clock pulses to one or to both ways of
4 said two way associative cache in response to a mode access signal;

5 an address circuit connected to simultaneously apply an address to each of said
6 sets of said two way associative cache;

7 an output multiplexer for selecting data from one of said sets of said associative
8 cache in response to a select signal identifying one of said ways of said associative
9 cache.

- 1 2. A system for accessing a two way associative data cache according to
2 claim 1 further comprising:

3 a tag array connected to be addressed by said address circuit for storing first
4 and second sets of tag signals corresponding to a corresponding set of data stored in
5 said first and second ways; and

6 first and second comparators connected to compare first and second output data
7 from said tag array with tag data derived from said address, thereby identifying one of
8 said ways of said associative caches containing data to be read, said one comparator
9 generating a select signal for said output multiplexer.

1 3. The system according to claim 1 wherein said control signal applies
2 clock pulses to both ways of said associate cache when the access time for reading
3 said data from one of said sets is less than a predetermined amount.

1 4. The system according to claim 1 wherein said access mode signal is
2 generated from prediction logic which predicts which of said sets contains said data.

1 5. The system according to claim 2 wherein said clock circuit receives data
2 from said comparator identifying which of said ways of said associative cache is to be
3 clocked.

1 6. The system according to claim 5 wherein said clock circuit receives an
2 access mode signal which indicates that both of said sets of associative cache are to be
3 clocked simultaneously.

1 7. The system according to claim 6 wherein said access signal is selected
2 based upon a need to conserve power by only applying clock pulses to one way of
3 said data cache, or to provide higher access speed to said data cache by applying clock
4 pulses to both ways of said data cache.

1 8. A system for accessing a data cache having at least two ways for storing
2 data at the same addresses, comprising:

3 a first and second tag memory for storing first and second sets of tags
4 identifying data stored in each of said ways;

5 a translation device for determining from a system address a tag identifying one
6 of said ways;

7 a first comparator for comparing tags in said address with a tag stored in said
8 first tag memory;

9 a second comparator for comparing a tag in said address with a tag stored in
10 said second tag memory;

11 a multiplexer for selecting output data from one of said ways in response to a
12 signal from one of said first and second comparators; and

13 a clock signal circuit for supplying clock signals to one or both of said ways
14 response to an access mode signal.

1 9. The system according to claim 8 wherein said access mode signal has a
2 first state which represents a power efficiency mode of operation.

1 10. The system according to claim 9 wherein said access mode signal has a
2 second state which represents a high access speed for said cache.

1 11. The system according to claim 9 wherein said access signal is in said first
2 state when said access speed is one half of a maximum access speed for said cache.

1 12. A method for accessing a set associative data cache comprising at least
2 two ways, comprising:

3 determining from an effective address tag associated with data stored in one of
4 said ways;

5 addressing said first and second ways with identical Line Index addresses
6 derived from said effective address;

7 addressing first and second tag memories with said Line Index address applied
8 to said first and second ways;

9 determining whether said first or second tag memories produce a tag identical
10 to said tag determined from said effective addresses; and

11 reading data from one of said ways in response to a first state of an access
12 signal, and reading data from both of said ways when said access signal has a second
13 state.

1 13. The method for accessing a set associative data cache according to claim
2 12 wherein said first state of said access signal is selected when said data cache is
3 read in a power conserving mode, and said second state of said access signal is
4 selected when said data cache is operated in a high speed access mode.

1 14. The method for accessing a set associative data cache according to claim
2 12 wherein said access mode signal controls a clock circuit that applies a clocking
3 signal to said first way in said first state, and applies clocking signals to both ways
4 when said access mode signal is in said second state.